DRIVER CIRCUIT CHARGING CHARGE NODE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] A claim for priority under 35 U.S.C. §119 is made to Korean Patent Application No. 10-2015-0144844 filed Oct. 16, 2015, in the Korean Intellectual Property Office, the entire contents of which are hereby incorporated by reference.

BACKGROUND

[0002] Example embodiments of inventive concepts described herein relate to a semiconductor circuit, and in more detail, to a driver circuit charging a charge node.

[0003] A memory device includes a plurality of memory cells. A plurality of memory cells is regularly disposed according to a specific pattern to reduce an area occupied by the memory cells. The memory cells disposed according to a regular pattern may be connected to conductive lines for accessing the memory cells.

[0004] The memory device is highly integrated as the number of memory cells connected to each conductive line increases and a distance between conductive lines becomes shorter. In this case, a resistive load and a capacitive load of each conductive line increase. When the resistive load and the capacitive load increase, a lot of time is required to drive a voltage of a conductive line to a target level, and thus an operating speed of the memory device may decrease. Accordingly, there are required a device and a method capable of driving each conductive line with a target voltage quickly even though the resistive load and capacitive load of each conductive line increase.

SUMMARY

[0005] Example embodiments of inventive concepts provide a driver circuit capable of reducing an occupied area and improving a driving speed.

[0006] According to example embodiments of inventive concepts, a driver circuit includes a clamp transistor, an amplification transistor, a bias transistor, and a charge circuit. The clamp transistor includes a clamp gate, a first clamp node, and a second clamp node connected to a charge node. The comparison voltage transistor includes a comparison voltage gate configured to receive a reference voltage, a first comparison voltage node configured to receive a first voltage, and a second comparison voltage node configured to output a comparison voltage. The amplification transistor includes an amplification gate connected to the charge node, a first amplification node connected to the second comparison voltage node of the comparison voltage transistor and configured to receive the comparison voltage, and a second amplification node connected to the clamp gate of the clamp transistor. The bias transistor includes a bias gate configured to receive a bias voltage, a first bias node connected to the clamp gate of the clamp transistor, and a second bias node configured to receive a second voltage. The charge circuit is one of configured to drain a current from the charge node through the clamp transistor and configured to supply a current to the charge node through the clamp transistor.

[0007] In example embodiments, the clamp transistor and the amplification transistor may be PMOS transistors, and the comparison voltage transistor and the bias transistor may be NMOS transistors.

[0008] In example embodiments, the first voltage may be a power supply voltage, and the second voltage may be a ground voltage.

[0009] In example embodiments, the clamp transistor and the amplification transistor may be NMOS transistors, and the comparison voltage transistor and the bias transistor may be PMOS type transistors.

[0010] In example embodiments, the first voltage may be a ground voltage, and the second voltage may be a power supply voltage.

[0011] In example embodiments, the driver circuit may further include an enable transistor connected between the clamp gate of the clamp transistor and the second amplification node of the amplification transistor, and the enable transistor may be configured to receive an enable signal and to be activated or inactivated based on the enable signal.

[0012] In example embodiments, the driver circuit may further include a voltage generator configured to supply a third voltage to the second clamp node of the clamp transistor.

[0013] In example embodiments, the amplification transistor may be configured to adjust a voltage of the clamp gate such that a voltage of the charge node reaches a target voltage.

[0014] In example embodiments, the reference voltage may be based on the target voltage of the charge node, a threshold voltage of the comparison voltage transistor, and a threshold voltage of the amplification transistor.

[0015] In example embodiments, the charge node may be connected to one of a word line and a bit line connected to memory cells.

[0016] According to example embodiments of inventive concepts, a driver circuit includes a clamp switch, a charge circuit, a comparison voltage generator, a single stage amplifier, and a current bias circuit. The clamp switch includes a gate configured to receive a clamp voltage, a first node, and a second node connected to a charge node. The charge circuit is connected to the first node of the clamp switch. The charge circuit is at least one of configured to drain a current from the charge node through the clamp switch and configured to supply a current to the charge node through the clamp switch. The comparison voltage generator is configured to output a comparison voltage. The single stage amplifier is configured to amplify a difference between the comparison voltage and a voltage of the charge node. The single stage amplifier is configured to output the clamp voltage as the amplification result. The current bias circuit is connected to the gate of the clamp switch. The current bias circuit is configured to adjust the amount of current flowing to a ground node to which a ground voltage is supplied through the comparison voltage generator, the single stage amplifier, and the bias circuit.

[0017] In example embodiments, the single stage amplifier may include a transistor including a gate connected to the charge node, a first node connected to the comparison voltage generator, and a second node connected to the gate of the clamp switch.

[0018] In example embodiments, the charge circuit may include a first transistor connected between the first node of the clamp switch and a first voltage node to which a first